MANUFACTURER DOCUMENT PACKAGE

Manufacturer's Manual

Reference package for procurement and maintenance review

TRICONEX

3006

MAIN PROCESSOR MODULE

Selected official pages follow this cover with source pagination retained.

REFERENCE PACKAGE

Source: Planning and Installation Guide for Tricon v9-v10 Systems

OFFICIAL MANUFACTURER DOCUMENT

Assembly 9700077-012

Main Processor Modules

A Tricon chassis houses three Main Processor Modules, each serving one channel (also referred to as a *leg*) of the controller. Each processor independently communicates with its I/O subsystem and executes the control program. The three MP Modules compare data and the control program at regular intervals. Each Main Processor operates autonomously with no shared clocks, power regulators, or circuitry. Processor specifications are listed in the specifications table for each MP.

A high-speed proprietary bus system called TriBus provides these functions: interprocessor communications, hardware majority voting of all digital input data, and comparison of control program variables. TriBus uses a fully isolated, serial communication channel operating at 4 megabits per second. A direct memory access controller manages the synchronization, transfer, voting and data correction independent of the control program or executive software.

DRAM (dynamic random-access memory) is used for control program, sequence-of-events data, I/O data, diagnostics, and communication buffers. SRAM (static random-access memory) is used for the defined program retentives and configuration of disabled points. Memory is regularly validated by the TriBus hardware-voting circuitry.

Sequence of Events Capability

Main Processors work with the communication modules to provide the Tricon controller with sequence-of-events (SOE) capability. During each scan, the Main Processors inspect designated discrete (Boolean) variables for changes of state known as events. When an event occurs, the Main Processors save the current state of the variable and includes a time stamp in an area of memory called a buffer which is a part of an SOE block. You can configure the SOE blocks using TriStation and retrieve the event data with software such as the Triconex SOE Recorder.

Compatible Modules

This table identifies the compatibility of Main Processor modules with Tricon versions. All the communication and I/O modules are compatible with v9—v10.x MPs.

Table 7 Compatibility of Main Processor Modules

Main Processor Model	Compatible Tricon Versions
3006 and 3007	v9.0—v9.5.x, and v9.51.x
3008	v9.6—v10.x

Main Processor Front Panel

This figure depicts the Main Processor front panels for models 3006, 3007, and 3008.

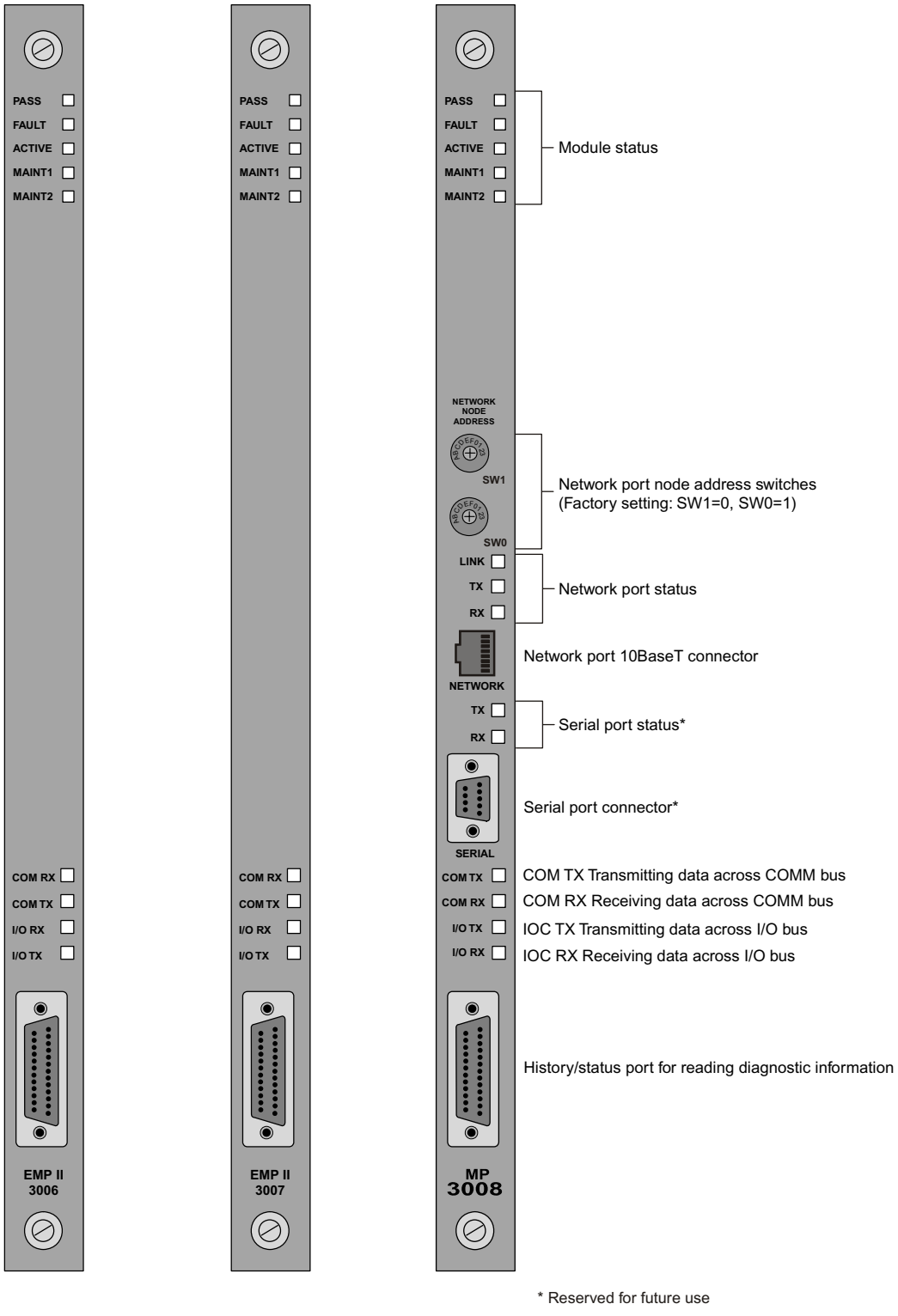

Figure 14 3006, 3007, and 3008 Main Processor Front Panels

Table 8 3008 Main Processor Specifications

Feature	Description
Serial port	For diagread diagnostic analysis Optically isolated RS-232 interface on one 25-pin connector 500 VDC isolation
Communication processor	Motorola MPC860, 50 MHz, 32-bit
Communication interface	
Protocol	RS-485
Baud rate	2 megabits per second
I/O interface	
Protocol	RS-485
Baud Rate	375 kilobits per second
Logic power	10 W

3006 and 3007 Main Processor Architecture

This figure depicts the model 3006 and 3007 Main Processor architecture, which can be used with Tricon v9.0—v9.5 systems. They have the same architecture and specifications, except for SRAM, which is 2 megabytes for the 3006 and 1 megabyte for the 3007.

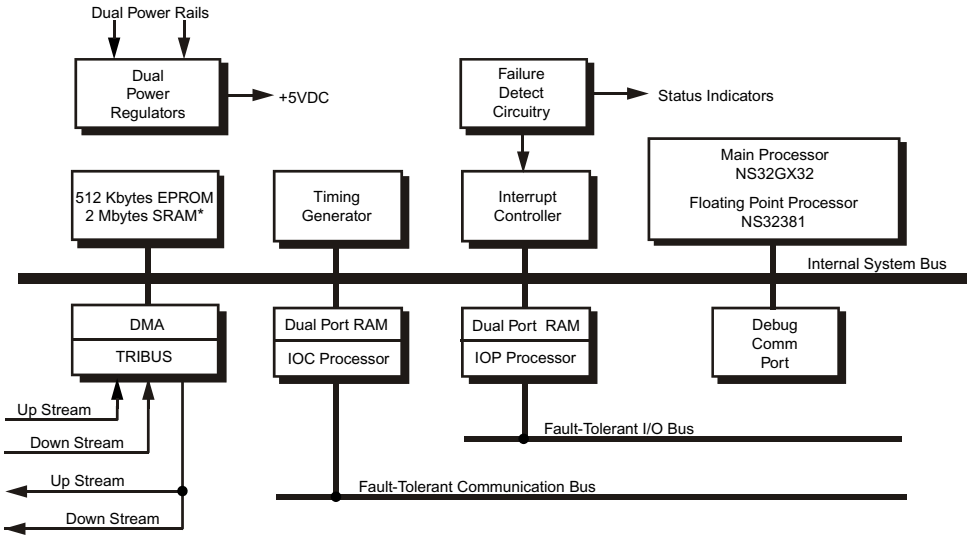

Figure 16 3006 and 3007 Main Processor Architecture

3006 and 3007 Specifications

This table lists the specifications for the 3006 and 3007 Main Processors, which can be used with Tricon v9.0—v9.5 systems.

Table 9 3006 and 3007 Main Processor Specifications

Feature	Specification
Central processor	National NS32GX32, 32 bits, 25 MHz
Math co-processor	National NS32381, 32 bits, 25 MHz
EPROM memory	512KB
SRAM	Model 3006: 2 MB Model 3007: 1 MB
Clock calendar	Time and date Battery backup Typical drift: ±2 seconds per day Maximum drift: ±8.6 seconds per day
TriBus	4 megabits per second, 16-bit DMA
Serial port	For Diagread diagnostic analysis Optically isolated RS-232 interface on one 25-pin connector 500 VDC isolation
Communication processor	Intel 80C152 32 KB EPROM, 64K shared memory interface 16 MHz
Communication Interface	
Protocol Baud rate	RS-485 2 megabits per second
I/O processor	Intel 80C31 12 MHz 32 KB EPROM 64K Shared Memory Interface
I/O interface	
Protocol Baud Rate	RS-485 375 kilobits per second
Logic power	15 W

Slot Key Numbers

This table lists the keys for Main Processors and the COM (used for TCM, EICM, or NCM) slots.

Table 73 Main Processor, COM, and Blank Slot Keys

Model	Module Name	Top Key	Bottom Key
3008	Main Processor (MP) Module	007	002
3006, 3007	Main Processor (MP) Module	007	007
	COM Slot (TCM. EICM, or NCM)	001	003
	Blank Logical Slot[1]	001	008

1. Use this key combination or part number 2000508-001 to prevent the insertion of modules into any unused slots in your controller.

This table lists the keys for I/O and communication module slots.

Table 74 I/O and Communication Module Slot Keys

Model	Module Name	Top Key	Bottom Key
3501E/T	115 VAC/DC Digital Input (TMR)	004	004
3502E	48 VAC/DC Digital Input with Self-Test (TMR)	004	005
3503E	24 VAC/DC Digital Input with Self-Test (TMR)	004	006
3504E	24 VDC /48 VDC High Density Digital Input (TMR)	004	007
3505E	24 VDC Low Threshold Digital Input with Self-Test (TMR)	004	006
3510	Pulse Input, AC Coupled (TMR)	004	001
3511	Pulse Input, AC Coupled (TMR)	004	001
3515	Pulse Totalizer Input	004	002
3564	24 VDC Digital Input (Single)	004	006
3601E/T	115 VAC Digital Output (TMR)	006	004
3603B	120 VDC Digital Output (TMR), non-commoned	006	006
3603E/T	120 VDC Digital Output (TMR), commoned	006	006
3604E	24 VDC Digital Output (TMR)	006	007
3607E	48 VDC Digital Output (TMR)	006	003
3611E	115 VAC Supervised Digital Output (TMR)	005	002
3613E	120 VDC Supervised Digital Output (TMR)	005	005
3614E	24 VDC Supervised Digital Output (TMR)	005	004
3615E	24 VDC Low-Power Supervised Digital Output (TMR)	005	004
3617E	48 VDC Supervised Digital Output (TMR)	005	003
3623/T	120 VDC Supervised Digital Output (TMR)	005	005

Table 85 3006 Main Processor Status Indicator Conditions

Pass	Fault	Active	Maint1	Maint2	Description	Action
Green steady	No light	Yellow blinking	No light	No light	The module is operating normally. The ACTIVE indicator blinks once per scan when executing a control program.	No action is required.
Green steady	No light	No light	—[1]	—	No control program has been loaded into the MP, or a control program has been loaded into the MP but has not been started. This state also exists in a module that has just been installed and is being educated by the other MPs.	If the ACTIVE indicator does not go on within a few minutes, the module is faulty and must be replaced.
Off	Red steady	No light	Red blinking	No light	The MP is re-educating. Allow six minutes for the PASS indicator to turn on, followed by the ACTIVE indicator.	No action is required.
Off	Red steady	—	Red steady	—	The module has failed.	Replace the module.
Off	Off	—	—	—	The indicators/signal circuitry on the module are malfunctioning.	Replace the module.
Green steady	Off	—	No light	Red steady	The MP soft error count is very high.	Replace the module at the first opportunity.

1. This symbol (—) means the indicator is not important for this condition.

MP Communication Indicators

The Main Processors include indicators that identify the status of communication across the COMM bus and I/O bus. The 3008 Main Processor has additional indicators that identify the status of network communication.

Table 86 Communication Indicators for Main Processors

RX	TX	Description	Action
Yellow Blinking	Yellow Blinking	Normal response. MPs are communicating with the I/O and communication modules.	No action is required.
No light	No light	Problem: MPs are not communicating with modules.	Replace the module.