Module and Application Description

PROCONTROL P

Analog Control

Control Module

For Analog Control Functions with Continuous Output, 1- and 2-fold

1KGD 003 930, Edition 08/05

83SR07-E/R1210

Application

The module is used for stored-program analog control of one or two process variables. The module is provided with two continuous outputs for output of the correcting variables. The following types of actuators can be controlled:

- electrohydraulic actuators
- electropneumatic actuators
- electric-motor-powered drives

The drives are positioned either locally at the transducer or in case of electric-motor-powered actuators, in a continuously operating power electronics system. It is also possible to supplement the single variable analog controls by a higher-level master control system.

The module is intended for use in connection with the process operator station.

The module incorporates the function blocks for implementing continuous single variable controllers. Additional function blocks are available for signal conditioning.

In the analog control mode, the module is used with fixed cycle times. This is 100 ms for one actuator and 200 ms for two actuators.

The cycle time is specified by means of function block KON, which is the first block to appear in the structure.

The module incorporates two hardware process interfaces for the power controller units and the process.

Features

The module address is set automatically by plugging the module into the PROCONTROL station.

The telegrams received via the bus are checked by the module for error-free transfer by means of their parity bits.

The telegrams sent by the module to the bus are provided with parity bits to ensure error-free transfer.

The user program is stored in a non-volatile memory (EEPROM). It can be loaded and changed from the PDDS via the bus.

The module is ready for operation as soon as a valid user list is loaded.

For communication with the process and the switchgear, the module requires the following voltage:

USA/USB operating voltage +24 V

internally branched into the voltages:

UK1	supply of contacts of process interface 1
UK2	supply of contacts of process interface 2
S11/S13	supply of transducer of process interface 1
S21/S23	supply of transducer of process interface 2

These voltages are short-circuit-proof and designed to prevent any interaction.

The operating voltages and the external logic signals are related to reference conductor Z.

The following annunciations are indicated on the front panel of the module by LEDs:

ST	disturbance
SG	module disturbance

The LED ST signals any disturbance in the module and in data communication with the module.

The LED SG signals module disturbances only.

Module design

The module comprises:

- Process interfaces
- Station bus interface
- Processing section

Process interface

In the process interfaces the process signals are adapted to the internal signal level of the module.

Station bus interface

In the station bus interface the module signals are adapted to the bus. This essentially involves a parallel/serial conversion.

Processing section

In order to process the signals coming from the process and the bus, the module is provided with a microprocessor which co-operates with the following memory areas via an internal bus of the module:

Contents	Storage medium
Operating program	EPROM
Function blocks	EPROM
User program (structure, address, parameters, limit value and simulation list)	EEPROM
User program (structure, address, parameter, limit value and simulation list)	RAM
History values	RAM
Current module input and output signals (shared memory)	RAM

The operating program enables the microprocessor to perform the operations of the module.

The function block memory contains the software modules needed to implement the various functions.

All function blocks together with their inputs and outputs can be called by the user via the Programming, Diagnostic and Display System (PDDS).

The user program memory contains the following information:

- how the function blocks are interconnected,
- which module inputs and outputs are allocated to the inputs and outputs of the function blocks,
- which constants are specified to the individual inputs of the function blocks,
- which parameters are specified to the individual inputs of the function blocks,
- which plant signals are allocated to the module inputs and outputs,
- which function blocks serve the process interfaces,
- which limit values are allocated to the analog values,
- which calculated function results, module input and output signals are simulated.

This information is specified by the user according to the plant involved.

The complete user program is filed in an EEPROM for normal operation. For optimizing purposes, it is possible to work with a modified copy of the user program in RAM, which must be taken over into the EEPROM upon completion of optimization.

Settings can be either preset by the user directly at the appropriate function block inputs or specified in a separate parameter list.

When limit signals are generated by means of function block GRE, the limit values (4 per GRE) are specified in a limit values list.

Parameter and limit value lists can be changed (on-line) at anytime during operation. In this case they are stored in the RAM or EEPROM, depending on whether they are assigned to the RAM or EEPROM mode.

Data exchange of the module with the bus system is performed via the memory for the module input and output signals. It buffers the signals.

Structuring

During structuring module inputs and outputs are allocated to the neutral inputs and outputs of the function blocks or constants and parameters or output from other function blocks (calculated function results) are specified to the function block inputs. Structuring is performed on the basis of data supplied by the user in the form of a so-called structure list.

The following limit values of the module shall be observed for structuring:

- max. number of module inputs 287
- max. number of simulated calculated function results, module inputs and outputs 32
- max. number of module outputs 223
- max. number of calculated function results 255
- max. number of timers 136
- max. number of parameters 80
- max. number of limit value sets 16
- max. number of drive control functions ASP 2
- max. number of lines in the structure list 2823
- length of historic values list (bytes) 1024
- design of shared memory (see “Addressing”)

A line is an entry on the PDDS.

For the precise procedure of structuring the function blocks, please refer to the respective function block descriptions.

Addressing

General

The signal exchange between the module and the bus system is performed via a shared memory. Incoming telegrams to be received by the module and calculated function results intended to leave the module are buffered in the shared memory.

The shared memory has send registers for telegrams to be transmitted and receive registers for telegrams to be received. The register numbers 0 to 63 are defined as send registers and the register numbers 64 to 199 as receive registers.

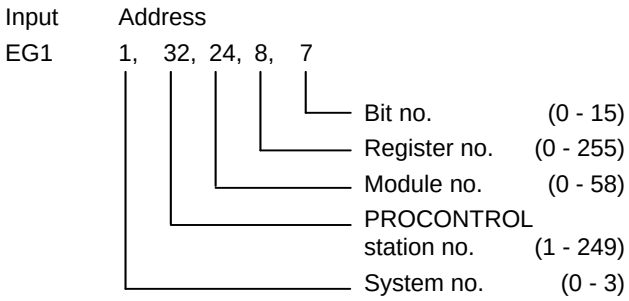
The module input and output signals are allocated to the shared memory registers as specified by the user via the PDDS.

The user data are contained in address lists.

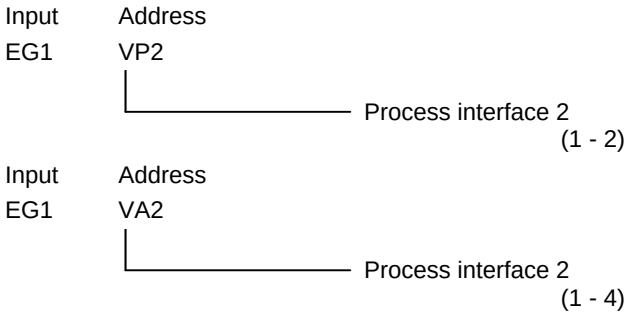
Address list for module inputs

In the address list for module inputs, each module input is assigned the send-location address or the process interface of the signal to be received.

In the case of module inputs that receive their signals over the bus, addressing is done by allocating the send-location address to EGn, e.g.:



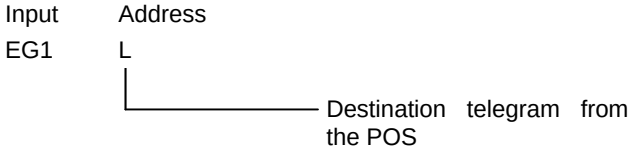
In the case of module inputs that receive their signals via the process interface, addressing is done by allocating the process interface to EGn. In this case, a distinction is to be made between contact inputs (VPn) and analog inputs (VAn), e.g.:



VAn allocation:

VA1:	Analog input	E11 of	process interface	1
VA2:	Analog input	E21 of	process interface	2
VA3:	Analog input	E13 of	process interface	1
VA4:	Analog input	E23 of	process interface	2

In the case of module inputs which receive their signal from the process operator station (POS), addressing is done by allocating L to EGn, e.g.:



The address list for inputs is translated by the PDDS into two internal lists, the “Bus address list“ and the “Module inputs allocation list“.

The bus address list contains, for all the telegrams to be used by the module, the send-location address and the receive register number.

Telegrams received, whose addresses are contained in the bus address list, are registered in the receive register of the shared memory. Telegrams received, whose addresses are not contained in the bus address list, are ignored by the module.

The "Module inputs allocation list" contains the associated receive register number for each module input and, in the case of binary values, the bit position.