MANUFACTURER DOCUMENT PACKAGE

Manufacturer's Manual

Reference package for procurement and maintenance review

INVENSYS TRICONEX

3008

TMR MAIN PROCESSOR MODULE

Used with the applicable Tricon v9-v10 system configuration.

REFERENCE PACKAGE

Selected official pages follow this cover with source pagination retained.

OFFICIAL DOCUMENT

Invensys 9700077-012, February 2009

Main Processor Modules

A Tricon chassis houses three Main Processor Modules, each serving one channel (also referred to as a *leg*) of the controller. Each processor independently communicates with its I/O subsystem and executes the control program. The three MP Modules compare data and the control program at regular intervals. Each Main Processor operates autonomously with no shared clocks, power regulators, or circuitry. Processor specifications are listed in the specifications table for each MP.

A high-speed proprietary bus system called TriBus provides these functions: interprocessor communications, hardware majority voting of all digital input data, and comparison of control program variables. TriBus uses a fully isolated, serial communication channel operating at 4 megabits per second. A direct memory access controller manages the synchronization, transfer, voting and data correction independent of the control program or executive software.

DRAM (dynamic random-access memory) is used for control program, sequence-of-events data, I/O data, diagnostics, and communication buffers. SRAM (static random-access memory) is used for the defined program retentives and configuration of disabled points. Memory is regularly validated by the TriBus hardware-voting circuitry.

Sequence of Events Capability

Main Processors work with the communication modules to provide the Tricon controller with sequence-of-events (SOE) capability. During each scan, the Main Processors inspect designated discrete (Boolean) variables for changes of state known as events. When an event occurs, the Main Processors save the current state of the variable and includes a time stamp in an area of memory called a buffer which is a part of an SOE block. You can configure the SOE blocks using TriStation and retrieve the event data with software such as the Triconex SOE Recorder.

Compatible Modules

This table identifies the compatibility of Main Processor modules with Tricon versions. All the communication and I/O modules are compatible with v9—v10.x MPs.

Table 7 Compatibility of Main Processor Modules

Main Processor Model	Compatible Tricon Versions
3006 and 3007	v9.0—v9.5.x, and v9.51.x
3008	v9.6—v10.x

Main Processor Front Panel

This figure depicts the Main Processor front panels for models 3006, 3007, and 3008.

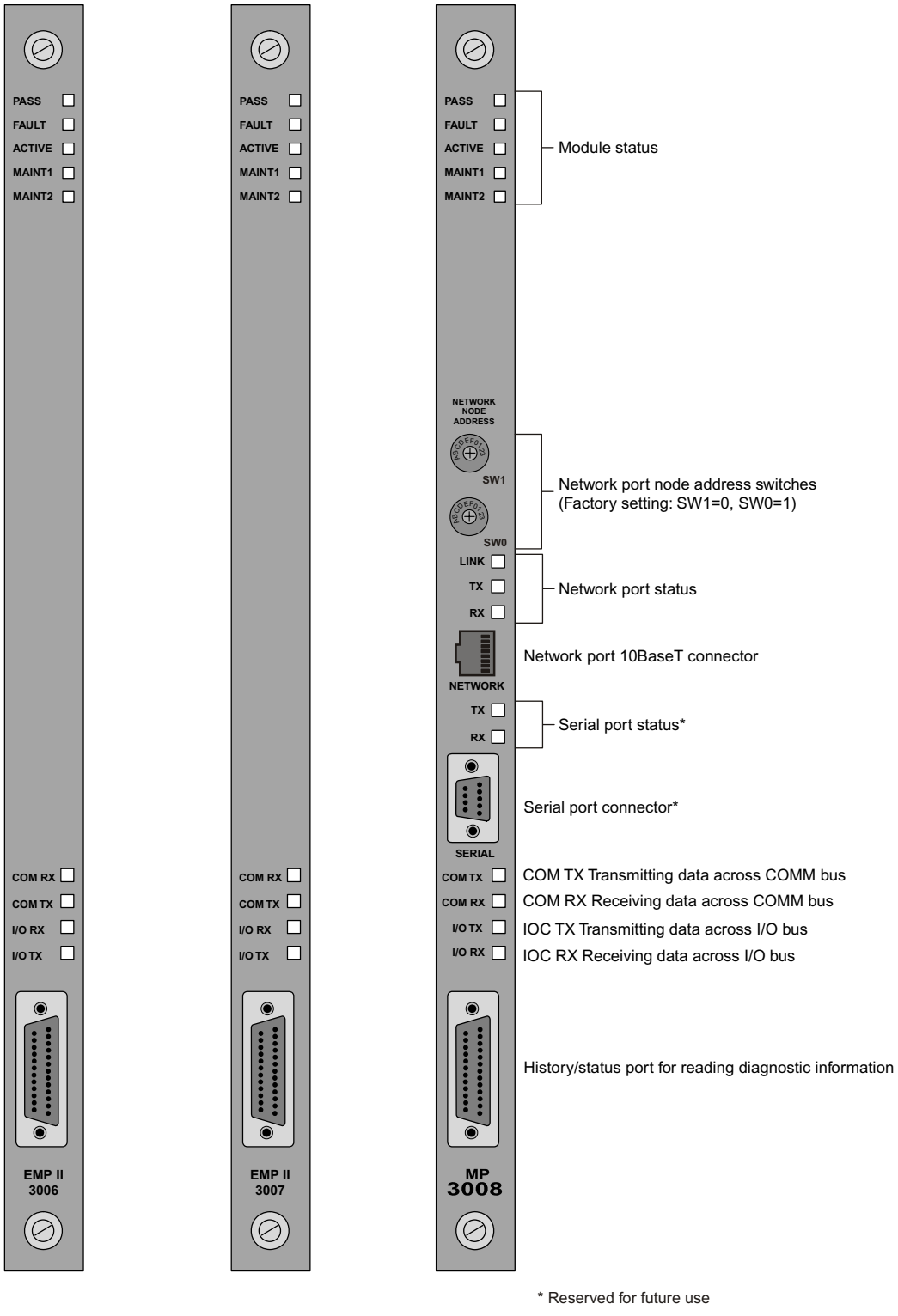

Figure 14 3006, 3007, and 3008 Main Processor Front Panels

3008 Main Processor Architecture

This figure depicts the model 3008 Main Processor architecture, which can be used with Tricon v9.6 and later systems.

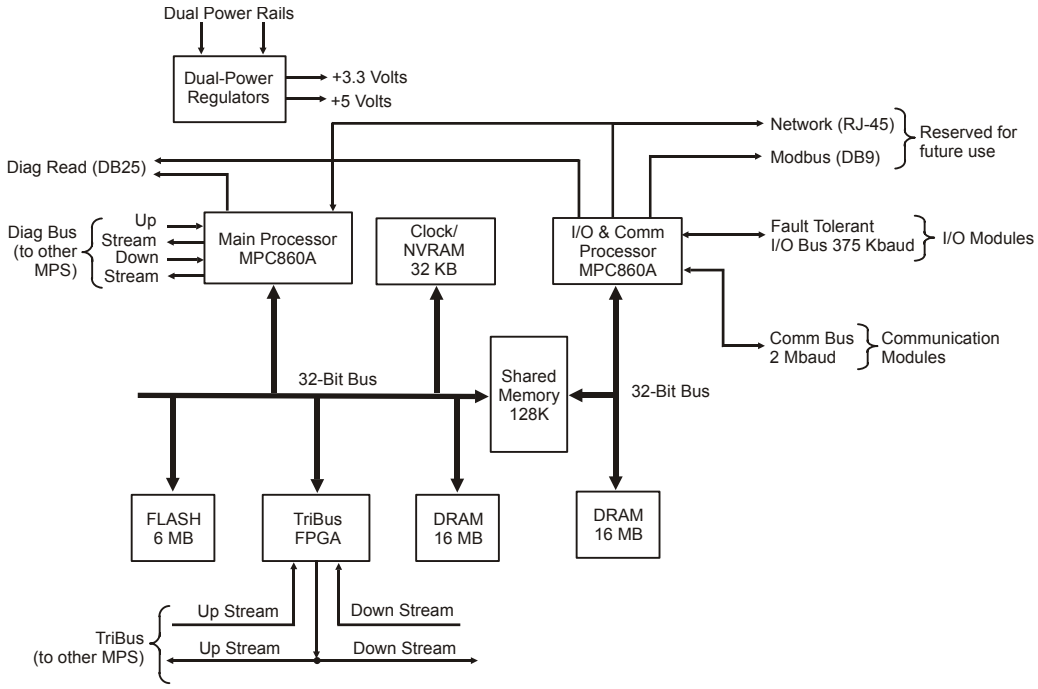

Figure 15 3008 Architecture

3008 Specifications

This table lists the specifications for the model 3008 Main Processor Module, which is available with Tricon v9.6 and later systems.

Table 8 3008 Main Processor Specifications

Feature	Description
Main processor	Motorola MPC860, 32-bit, 50 MHz
Memory	16 MB DRAM (without battery back-up) 32 KB SRAM (with battery back-up) 6 MB Flash PROM
TriClock	Time and date Battery back-up Typical drift: ±2 seconds/day Maximum drift: ±2.16 seconds/day
TriBus	25 megabits/second 32-bit CRC-protected 32-bit DMA, fully isolated

Table 8 3008 Main Processor Specifications

Feature	Description
Serial port	For diagread diagnostic analysis Optically isolated RS-232 interface on one 25-pin connector 500 VDC isolation
Communication processor	Motorola MPC860, 50 MHz, 32-bit
Communication interface	
Protocol	RS-485
Baud rate	2 megabits per second
I/O interface	
Protocol	RS-485
Baud Rate	375 kilobits per second
Logic power	10 W

3006 and 3007 Main Processor Architecture

This figure depicts the model 3006 and 3007 Main Processor architecture, which can be used with Tricon v9.0—v9.5 systems. They have the same architecture and specifications, except for SRAM, which is 2 megabytes for the 3006 and 1 megabyte for the 3007.

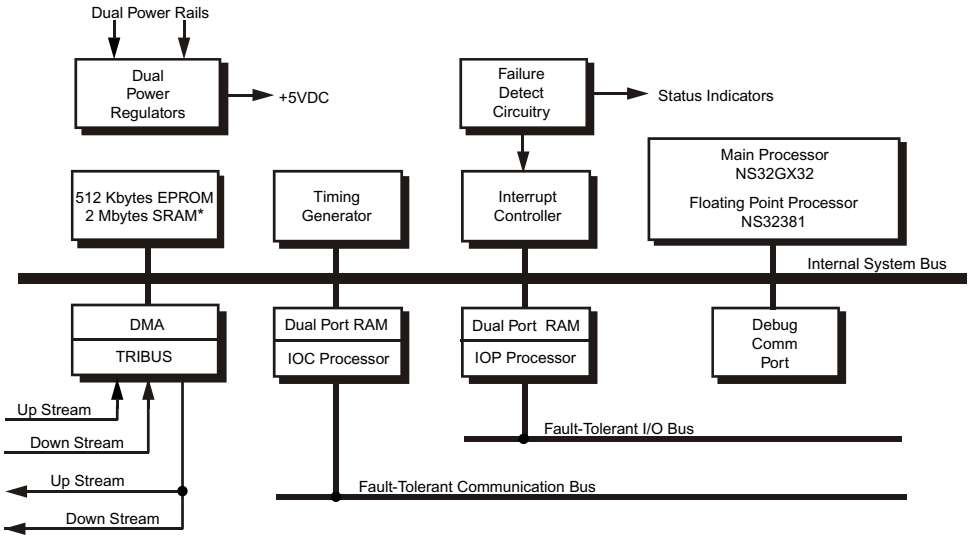

Figure 16 3006 and 3007 Main Processor Architecture

Slot Key Numbers

This table lists the keys for Main Processors and the COM (used for TCM, EICM, or NCM) slots.

Table 73 Main Processor, COM, and Blank Slot Keys

Model	Module Name	Top Key	Bottom Key
3008	Main Processor (MP) Module	007	002
3006, 3007	Main Processor (MP) Module	007	007
	COM Slot (TCM. EICM, or NCM)	001	003
	Blank Logical Slot[1]	001	008

1. Use this key combination or part number 2000508-001 to prevent the insertion of modules into any unused slots in your controller.

This table lists the keys for I/O and communication module slots.

Table 74 I/O and Communication Module Slot Keys

Model	Module Name	Top Key	Bottom Key
3501E/T	115 VAC/DC Digital Input (TMR)	004	004
3502E	48 VAC/DC Digital Input with Self-Test (TMR)	004	005
3503E	24 VAC/DC Digital Input with Self-Test (TMR)	004	006
3504E	24 VDC /48 VDC High Density Digital Input (TMR)	004	007
3505E	24 VDC Low Threshold Digital Input with Self-Test (TMR)	004	006
3510	Pulse Input, AC Coupled (TMR)	004	001
3511	Pulse Input, AC Coupled (TMR)	004	001
3515	Pulse Totalizer Input	004	002
3564	24 VDC Digital Input (Single)	004	006
3601E/T	115 VAC Digital Output (TMR)	006	004
3603B	120 VDC Digital Output (TMR), non-commoned	006	006
3603E/T	120 VDC Digital Output (TMR), commoned	006	006
3604E	24 VDC Digital Output (TMR)	006	007
3607E	48 VDC Digital Output (TMR)	006	003
3611E	115 VAC Supervised Digital Output (TMR)	005	002
3613E	120 VDC Supervised Digital Output (TMR)	005	005
3614E	24 VDC Supervised Digital Output (TMR)	005	004
3615E	24 VDC Low-Power Supervised Digital Output (TMR)	005	004
3617E	48 VDC Supervised Digital Output (TMR)	005	003
3623/T	120 VDC Supervised Digital Output (TMR)	005	005

Main Processor Status Indicators

The status indicators identify the processing state for the Main Processors. A fault indicator indicates that the processor has an internal fault.

Table 84 3008 Main Processor Status Indicator Conditions

Pass	Fault	Active	Maint1	Maint2	Description	Action
Green steady	No light	Yellow blinking	No light	No light	The module is operating normally. The Active indicator blinks once per scan when executing an application.	No action is required.
No light	Red steady	— [1]	—	—	The module has failed.	Replace the module.
No light	No light	—	—	—	The indicators/signal circuitry on the module are malfunctioning.	Replace the module.
Green steady	No light	No light	Red blinking	No light	The MP is re-educating. Allow 10 minutes for the PASS indicator to turn on, followed by the ACTIVE indicator	No action is required.
Green steady	No light	Yellow blinking	Red steady	No light	Minor Fault in noncritical portion of MP, such as the battery voltage, clock calendar not running, or temperature mismatch. For v10 and later, this may indicate that the module has excessively reset or re-educated in the last 100 days.	Extract a Tricon Event Log file and send it to the Invensys GCS for analysis.
Green steady	No light	Yellow blinking	No light	Red steady	The MP printed circuit board temperature is greater than 183° F (84° C) or less than 32° F (0° C).	Verify Temperature conditions within cabinet are normal. If so Replace the module.
No light	Red steady	No light	Red blinking	Red blinking	MP firmware does not match other MPs.	Replace the module with one that has matching firmware.

1. This symbol (—) means the indicator is not important for this condition.