MANUFACTURER DOCUMENT PACKAGE

Manufacturer's Manual

Selected official pages for procurement and maintenance review

PRODUCT BRAND

Siemens

PRODUCT MODEL

6ES7215-1AF40-0XB0

CPU 1215FC Fail-Safe Controller. Relevant section pages: 2, 5, 13, 14, 160, 161, 162, 163, 164, 165, 166, 167. Adjacent model text on shared pages is outside this product reference.

OFFICIAL SOURCE

S7-1200 Functional Safety Manual; 02/2015

Source: Siemens 02/2015. Original manufacturer pages follow this cover.

Historical manufacturer technical reference, 02/2015. Integrated CPU I/O is standard, not fail-safe. This excerpt is not a complete safety installation, programming or acceptance manual.

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Amikon Limited prepared this independent reference package. Selected manufacturer pages follow with their original content and pagination visible.

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This manual contains notices you have to observe in order to ensure your personal safety, as well as to prevent damage to property. The notices referring to your personal safety are highlighted in the manual by a safety alert symbol, notices referring only to property damage have no safety alert symbol. These notices shown below are graded according to the degree of danger.

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indicates that death or severe personal injury **will** result if proper precautions are not taken.

⚠ WARNING

indicates that death or severe personal injury **may** result if proper precautions are not taken.

⚠ CAUTION

indicates that minor personal injury can result if proper precautions are not taken.

NOTICE

indicates that property damage can result if proper precautions are not taken.

If more than one degree of danger is present, the warning notice representing the highest degree of danger will be used. A notice warning of injury to persons with a safety alert symbol may also include a warning relating to property damage.

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The product/system described in this documentation may be operated only by **personnel qualified** for the specific task in accordance with the relevant documentation, in particular its warning notices and safety instructions. Qualified personnel are those who, based on their training and experience, are capable of identifying risks and avoiding potential hazards when working with these products/systems.

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Documentation and information

S7-1200 and STEP 7 provide a variety of documentation and other resources for finding the technical information that you require.

- The *S7-1200 Functional Safety Manual* presents an overview of the Siemens Safety software and fail-safe CPUs and SMs and a Getting Started configuration and programming example. However, the focus of the manual is the S7-1200 fail-safe SMs. SM installation, configuration, diagnostics, applications, and technical specifications are emphasized.

  The English version of the *S7-1200 Functional Safety Manual* is the authoritative (original) language for Functional Safety-related information. All translated manuals refer back to the English manual as the authoritative and/or original source. Siemens identifies the English manual as the authoritative and/or original source in the case of discrepancies between the translated manuals.

- The *Industrial Software, SIMATIC Safety - Configuring and Programming, Programming and Operating Manual* provides information that enables you to configure and program SIMATIC Safety fail-safe systems. In addition, you will obtain information on acceptance testing of a SIMATIC Safety fail-safe system. Before configuring and programming an actual live fail-safe operation, it is essential that you refer to this manual.

- The *S7-1200 Programmable Controller System Manual* provides specific information about the operation, programming, and the specifications for the complete S7-1200 product family. In addition to the system manual, the *S7-1200 Easy Book* provides a more general overview to the capabilities of the S7-1200 family.

- The *S7-1200 Functional Safety Manual; SIMATIC, Industrial Software, SIMATIC Safety - Configuring and Programming, Programming and Operating Manual; S7-1200 Programmable Controller System Manual*; and the *S7-1200 Easy Book* are available as electronic (PDF) manuals. The electronic manuals can be downloaded from the customer support web site and can also be found on the companion disk that ships with every S7-1200 CPU.

- The TIA portal STEP 7 online help information system provides immediate access to the conceptual information, specific instructions, and error code event IDs that describe the operation and functionality of the programming package and basic operation of SIMATIC CPUs.

- My Documentation Manager accesses the electronic (PDF) versions of the SIMATIC documentation set, including the system manual, the Easy Book, and the information system of STEP 7. With My Documentation Manager, you can drag and drop topics from various documents to create your own custom manual.

  The customer support entry portal (http://support.automation.siemens.com) provides a link to My Documentation Manager under mySupport.

- Siemens also provides online comprehensive support for your use of safety technology. A Safety Evaluation Tool assists you in determining required safety levels, Functional Examples guide you in your safety applications, and SITRAIN classes offer training in safety standards and products. Visit the following web sites to access these support activities:

  – Safety Evaluation Tool (http://www.siemens.com/safety-evaluation-tool)

  – Functional examples (http://www.siemens.com/safety-functional-examples)

  – SITRAIN (http://www.siemens.com/sitrain-safetyintegrated)

1.2 Hardware and software components

S7-1200 Fail-Safe CPUs and SMs

There are four fail-safe CPUs and three fail-safe signal modules (SM) in conjunction with the S7-1200 V4.1 or later release:

- CPU 1214FC DC/DC/DC
- CPU 1214FC DC/DC/RLY
- CPU 1215FC DC/DC/DC
- CPU 1215FC DC/DC/RLY
- SM 1226 F-DI 16 x 24 VDC
- SM 1226 F-DQ 4 x 24 VDC
- SM 1226 F-DQ 2 x Relay

An S7-1200 fail-safe system requires a fail-safe CPU and fail-safe SMs. The integrated I/O on the CPU is not fail-safe, but can be used to complete other control functions.

The S7-1200 standard signal modules (SM), communication modules (CM), and signal boards (SB) can be used in the same system with fail-safe SMs to complete your application control functions that do not require a rated Safety Integrity Level (SIL). Standard SMs that are supported for use with fail-safe SMs have the article numbers (6ES7 --- ---32 0XB0) or later.

The S7-1200 fail-safe CPUs do not support PROFIBUS or PROFINET distributed fail-safe I/O.

Required software components

You require one of the following software combinations:

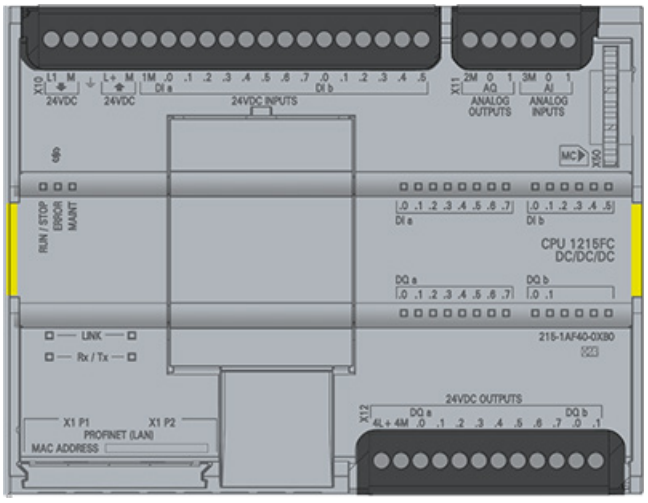
- STEP 7 Basic V13 SP1 or later with STEP 7 Safety Basic V13 SP1 or later
- STEP 7 Professional V13 SP1 or later with STEP 7 Safety Advanced V13 SP1 or later

STEP 7 Safety Advanced V13 SP1 or later and STEP 7 Safety Basic V13 SP1 or later are the configuration and programming software packages for the SIMATIC Safety fail-safe system. In both software packages, you receive the following:

- Support for configuring the fail-safe CPUs and SMs in the hardware and network editor of the TIA portal
- Support for creating the safety program using LAD and FBD and integrating error detection functions into the safety program
- Instructions for programming your safety program in LAD and FBD, which you are familiar with from the standard user programs
- Instructions for programming your safety program in LAD and FBD with special safety functions

1.3 S7-1200 Fail-Safe CPUs

The fail-safe CPU executes your safety program along with standard applications programs. Communication between the fail-safe CPU and the fail-safe signal modules is verified using the PROFIsafe protocol.



Safety program

You can create a safety program using the program editor. You can program fail-safe function blocks (FB) and functions (FC) in the Function Block Diagram (FBD) or Ladder Logic (LAD) programming languages and create fail-safe data blocks (DB).

The fail-safe system performs a dual execution using coded processing. The fail-safe system automatically performs safety checks and inserts additional fail-safe logic for error detection and error response when the safety program compilation occurs. This ensures the detection of failures and faults and appropriate execution of reactions to maintain the fail-safe system in the safe state or bring it to a safe state.

In addition to the safety program, you can run a standard user program on the fail-safe CPU. A standard program can coexist with a safety program in a fail-safe CPU. The fail-safe CPU protects the safety-related data of the safety program from the unintentional effects of the data of the standard user program.

⚠ WARNING

You cannot put an S7-1200 Fail-Safe system that provides safety-related functions into operation after installation or modification until after you successfully commission the safety-related functionality.

Death or serious personal injury and damage to machines and equipment may result if proper precautions are not taken.

An S7-1200 Fail-Safe system that provides both safety-related functions and standard (non safety-related) functions must not be put into operation in order to use the standard functions before you successfully commission the safety-related functions, even if all fail-safe signal modules go to the error state and thus remain safe.

A.2.3 CPU 1215FC

A.2.3.1 General specifications and features

Table A- 26 General

Technical data	CPU 1215FC DC/DC/Relay	CPU 1215FC DC/DC/DC
Article number	6ES7 215-1HF40-0XB0	6ES7 215-1AF40-0XB0
Dimensions W x H x D (mm)	130 x 100 x 75	
Shipping weight	550 grams	520 grams
Power dissipation	12 W	
Current available (SM and CM bus)	1600 mA max. (5 VDC)	
Current available (24 VDC)	400 mA max. (sensor power)	
Digital input current consumption (24 VDC)	4 mA/input used	

Table A- 27 CPU features

Technical data		Description
User memory (Refer to "General technical specifications (Page 132), "Internal CPU memory retention".)	Work	150 Kbytes
	Load	4 Mbytes, internal, expandable up to SD card size
	Retentive	10 Kbytes
On-board digital I/O		14 inputs/10 outputs
On-board analog I/O		2 inputs/2 outputs
Process image size		1024 bytes of inputs (I)/1024 bytes of outputs (Q)
Bit memory (M)		8192 bytes
Temporary (local) memory		• 16 Kbytes for startup and program cycle (including associated FBs and FCs) • 6 Kbytes for each of the other interrupt priority levels (including FBs and FCs)
Signal modules expansion		8 SMs max.
SB, CB, BB expansion		1 max.
Communication module expansion		3 CMs max.
High-speed counters		Up to 6 configured to use any built-in or SB inputs. (Refer to the *S7-1200 System Manual* for more information.) • 100/[1]80 kHz (Ia.0 to Ia.5) • 30/[1]20 kHz (Ia.6 to Ib.5)
Pulse outputs[2]		Up to 4 configured to use any built-in or SB outputs • 100 kHz (Qa.0 to Qa.3) • 30 kHz (Qa.4 to Qb.1)
Pulse catch inputs		14

Technical data	Description
Time delay interrupts	4 total with 1 ms resolution
Cyclic interrupts	4 total with 1 ms resolution
Edge interrupts	12 rising and 12 falling (16 and 16 with optional signal board)
Memory card	SIMATIC Memory Card (optional)
Real time clock accuracy	+/- 60 seconds/month
Real time clock retention time	20 days typ./12 days min. at 40 °C (maintenance-free Super Capacitor)

1 The slower speed is applicable when the HSC is configured for quadrature mode of operation.

2 For CPU models with relay outputs, you must install a digital signal board (SB) to use the pulse outputs.

Table A- 28 Performance

Type of instruction	Execution speed
Boolean	0.08 µs/instruction
Move Word	1.7 µs/instruction
Real math	2.3 µs/instruction

A.2.3.2 Timers, counters and code blocks supported

Table A- 29 Blocks, timers and counters supported by CPU 1215FC

Element		Description
Blocks	Type	OB, FB, FC, DB
	Size	64 Kbytes
	Quantity	Up to 1024 blocks total (OBs + FBs + FCs + DBs)
	Address range for FBs, FCs, and DBs	FB and FC: 1 to 65535 (such as FB 1 to FB 65535) DB: 1 to 59999
	Nesting depth	16 from the program cycle or startup OB 6 from any interrupt event OB
	Monitoring	Status of 2 code blocks can be monitored simultaneously
OBs	Program cycle	Multiple
	Startup	Multiple
	Time-delay interrupts	4 (1 per event)
	Cyclic interrupts	4 (1 per event)
	Hardware interrupts	50 (1 per event)
	Time error interrupts	1
	Diagnostic error interrupts	1
	Pull or plug of modules	1
	Rack or station failure	1
	Time of day	Multiple
	Status	1
	Update	1
	Profile	1

Element		Description
Timers	Type	IEC
	Quantity	Limited only by memory size
	Storage	Structure in DB, 16 bytes per timer
Counters	Type	IEC
	Quantity	Limited only by memory size
	Storage	Structure in DB, size dependent upon count type • SInt, USInt: 3 bytes • Int, UInt: 6 bytes • DInt, UDInt: 12 bytes

Table A- 30 Communication

Technical data	Description
Number of ports	2
Type	Ethernet
HMI device	4
Programming device (PG)	1
Connections	• 8 for Open User Communication (active or passive): TSEND_C, TRCV_C, TCON, TDISCON, TSEND, and TRCV • 3 for server GET/PUT (CPU-to-CPU) S7 communication • 8 for client GET/PUT (CPU-to-CPU) S7 communication
Data rates	10/100 Mb/s
Isolation (external signal to PLC logic)	Transformer isolated, 1500 VAC, for short term event safety only
Cable type	CAT5e shielded

Table A- 31 Power supply

Technical data		CPU 1215FC DC/DC/Relay	CPU 1215FC DC/DC/DC
Voltage range		20.4 VDC to 28.8 VDC	
Line frequency		--	
Input current (max. load)	CPU only	500 mA at 24 VDC	
	CPU with all expansion accessories	1500 mA at 24 VDC	
Inrush current (max.)		12 A at 28.8 VDC	
Isolation (input power to logic)		Not isolated	
Ground leakage, AC line to functional earth		-	
Hold up time (loss of power)		10 ms at 24 VDC	
Internal fuse, not user replaceable		3 A, 250 V, slow blow	

Table A- 32 Sensor power

Technical data	CPU 1215FC DC/DC/Relay	CPU 1215FC DC/DC/DC
Voltage range	L+ minus 4 VDC min.	
Output current rating (max.)	400 mA (short-circuit protected)	
Maximum ripple noise (<10 MHz)	Same as input line	
Isolation (CPU logic to sensor power)	Not isolated	

A.2.3.3 Digital inputs and outputs

Table A- 33 Digital inputs

Technical data	CPU 1215FC DC/DC/Relay	CPU 1215FC DC/DC/DC
Number of inputs	14	
Type	Sink/Source (IEC Type 1 sink)	
Rated voltage	24 VDC at 4 mA, nominal	
Continuous permissible voltage	30 VDC, max.	
Surge voltage	35 VDC for 0.5 sec.	
Logic 1 signal (min.)	15 VDC at 2.5 mA	
Logic 0 signal (max.)	5 VDC at 1 mA	
Isolation (field side to logic)	500 VAC for 1 minute	
Isolation groups	1	
Filter times	us settings: 0.1, 0.2, 0.4, 0.8, 1.6, 3.2, 6.4, 10.0, 12.8, 20.0 ms settings: 0.05, 0.1, 0.2, 0.4, 0.8, 1.6, 3.2, 6.4, 10.0, 12.8, 20.0	
HSC clock input rates (max.) (Logic 1 Level = 15 to 26 VDC)	100/80 kHz (Ia.0 to Ia.5) 30/20 kHz (Ia.6 to Ib.5)	
Number of inputs on simultaneously	14 inputs at 55 °C horizontal or 45 °C vertical	
Cable length (meters)	500 m shielded, 300 m unshielded, 50 m shielded for HSC inputs	

Table A- 34 Digital outputs

Technical data	CPU 1215FC DC/DC/Relay	CPU 1215FC DC/DC/DC
Number of outputs	10	10
Type	Relay, mechanical	Solid state - MOSFET (sourcing)
Voltage range	5 to 30 VDC or 5 to 250 VAC	20.4 to 28.8 VDC
Logic 1 signal at max. current	--	20 VDC min.
Logic 0 signal with 10 KΩ load	--	0.1 VDC max.
Current (max.)	2.0 A	0.5 A
Lamp load	30 W DC / 200 W AC	5 W
ON state resistance	0.2 Ω max. when new	0.6 Ω max.
Leakage current per point	--	10 µA max.
Surge current	7 A with contacts closed	8 A for 100 ms max.
Overload protection	No	No
Required external overload protection [4]	10 A maximum must be limited to any common	5 A maximum must be limited to any common
Isolation (field side to logic)	1500 VAC for 1 minute (coil to contact) None (coil to logic)	500 VAC for 1 minute
Isolation resistance	100 MΩ min. when new	--
Isolation between open contacts	750 VAC for 1 minute	--
Isolation groups	2	1
Isolation (group-to-group)	1500 VAC [1]	--
Inductive clamp voltage	--	L+ minus 48 VDC, 1 W dissipation
Switching delay (Qa.0 to Qa.3)	10 ms max.	1.0 µs max., off to on 3.0 µs max., on to off
Switching delay (Qa.4 to Qb.1)	10 ms max.	50 µs max., off to on 200 µs max., on to off
Maximum relay switching frequency	1 Hz	--
Pulse Train Output rate	Not recommended [2]	100 kHz (Qa.0 to Qa.3) [3], 2 Hz min. 20 kHz (Qa.4 to Qb.1) [3]
Lifetime mechanical (no load)	10,000,000 open/close cycles	--
Lifetime contacts at rated load	100,000 open/close cycles	--
Behavior on RUN to STOP	Last value or substitute value (default value 0)	
Number of outputs on simultaneously	10 outputs at 55 °C horizontal or 45 °C vertical	
Cable length (meters)	500 m shielded, 150 m unshielded	

1 Relay group-to-group isolation separates line voltage from SELV/PELV and separates different phases up to 250 VAC line to ground.

2 For CPU models with relay outputs, you must install a digital signal board (SB) to use the pulse outputs.

3 Depending on your pulse receiver and cable, an additional load resistor (at least 10% of rated current) may improve pulse signal quality and noise immunity.

4 External overload protection is to limit fire hazard. Overload can damage relay or transistor output.

A.2.3.4 Analog inputs and outputs

Table A- 35 Analog inputs

Technical data	Description
Number of inputs	2
Type	Voltage (single-ended)
Full-scale range	0 to 10 V
Full-scale range (data word)	0 to 27648
Overshoot range	10.001 to 11.759 V
Overshoot range (data word)	27649 to 32511
Overflow range	11.760 to 11.852 V
Overflow range (data word)	32512 to 32767
Resolution	10 bits
Maximum withstand voltage	35 VDC
Smoothing	None, Weak, Medium, or Strong See the table for step response (ms) for the analog inputs of the CPU.
Noise rejection	10, 50, or 60 Hz
Impedance	≥100 KΩ
Isolation (field side to logic)	None
Accuracy (25 °C / 0 to 55 °C)	3.0% / 3.5% of full-scale
Cable length (meters)	100 m, shielded twisted pair

Step response of built-in analog inputs of the CPU

Table A- 36 Step Response (ms), 0 V to 10 V measured at 95%

Smoothing selection (sample averaging)	Rejection frequency (Integration time)		
	60 Hz	50 Hz	10 Hz
None (1 cycle): No averaging	50 ms	50 ms	100 ms
Weak (4 cycles): 4 samples	60 ms	70 ms	200 ms
Medium (16 cycles): 16 samples	200 ms	240 ms	1150 ms
Strong (32 cycles): 32 samples	400 ms	480 ms	2300 ms
Sample time	**4.17 ms**	**5 ms**	**25 ms**

Sample time for the built-in analog ports of the CPU

Table A- 37 Sample time for built-in analog inputs of the CPU

Rejection frequency (Integration time selection)	Sample time
60 Hz (16.6 ms)	4.17 ms
50 Hz (20 ms)	5 ms
10 Hz (100 ms)	25 ms

Measurement ranges of the analog inputs for voltage of the CPU

Table A- 38 Analog input representation for voltage of the CPU

System		Voltage Measuring Range	
Decimal	**Hexadecimal**	**0 to 10 V**	
32767	7FFF	11.851 V	Overflow
32512	7F00		
32511	7EFF	11.759 V	Overshoot range
27649	6C01		
27648	6C00	10 V	Rated range
20736	5100	7.5 V	
34	22	12 mV	
0	0	0 V	
Negative values		Negative values are not supported	

Analog output specifications

Table A- 39 Analog outputs

Technical data	Description
Number of outputs	2
Type	Current
Full-scale range	0 to 20 mA
Full-scale range (data word)	0 to 27648
Overshoot range	20.01 to 23.52 mA
Overshoot range (data word)	27649 to 32511
Overflow range	see footnote [1]
Overflow range data word	32512 to 32767
Resolution	10 bits
Output drive impedance	≤500 Ω max.
Isolation (field side to logic)	None
Accuracy (25 °C / 0 to 55 °C)	3.0% / 3.5% of full-scale
Settling time	2 ms
Cable length (meters)	100 m, shielded twisted pair

[1] In an overflow condition, analog outputs will behave according to the device configuration properties settings. In the "Reaction to CPU STOP" parameter, select either: "Use substitute value" or "Keep last value".

Measurement ranges of the analog outputs for current of the CPU

Table A- 40 Analog output representation for current of the CPU

System		Current output range	
Decimal	**Hexadecimal**	**0 mA to 20 mA**	
32767	7FFF	See note 1	Overflow
32512	7F00	See note 1	
32511	7EFF	23.52 mA	Overshoot range
27649	6C01		
27648	6C00	20 mA	Rated range
20736	5100	15 mA	
34	22	0.0247 mA	
0	0	0 mA	
Negative values		Negative values are not supported	

1 In an overflow condition, analog outputs will behave according to the device configuration properties settings. In the "Reaction to CPU STOP" parameter, select either: "Use substitute value" or "Keep last value".