MANUFACTURER DOCUMENT PACKAGE

Manufacturer's Manual

Selected official pages for procurement and maintenance review

PRODUCT BRAND

Siemens

PRODUCT MODEL

6ES7414-1XG02-0AB0

CPU 414-1 Central Processing Unit. Relevant section pages: 5, 6, 7, 11, 12. Adjacent model text on shared pages is outside this product reference.

OFFICIAL SOURCE

S7-400, M7-400 Supplement to the Documentation; 1998; C79000-Z7076-C417-06

Siemens original documentation and product reference

Historical supplement: CPU 414-1 notes apply from release level 02. This excerpt is not a complete electrical or installation manual; verify the supplied unit release.

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Amikon Limited prepared this independent reference package. Selected manufacturer pages follow with their original content and pagination visible.

SIEMENS

SIMATIC S7

Supplement to the Documentation

C79000-Z7076-C417-06

6ES7498-8AA02-8BA0

S7-400, M7-400 Programmable Controllers

This Supplement contains **additional information** about the products. It is a separate component and should be considered **more up-to-date** than the information in the manuals and catalogs if uncertainties arise.

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We have checked the contents of this manual for agreement with the hardware and software described. Since deviations cannot be precluded entirely, we cannot guarantee full agreement. However, the data in this manual are reviewed regularly and any necessary corrections included in subsequent editions. Suggestions for improvement are welcomed.

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Supplement to the Documentation

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The information in this supplement regarding the properties of CPUs relates to the following CPUs with their specified release levels.

CPU	Order Number	From Release Level
CPU 412-1	6ES7 412-1XF02-0AB0	02
CPU 413-1	6ES7 413-1XG02-0AB0	01
CPU 413-2 DP	6ES7 413-2XG02-0AB0	01
CPU 414-1	6ES7 414-1XG02-0AB0	02
CPU 414-2 DP, 128 Kbytes	6ES7 414-2XG02-0AB0	02
CPU 414-2 DP, 384 Kbytes	6ES7 414-2XJ01-0AB0	02
CPU 416-1	6ES7 416-1XJ02-0AB0	02
CPU 416-2 DP, 0.8 Mbytes	6ES7 416-2XK01-0AB0	02
CPU 416-2 DP, 1.6 Mbytes	6ES7 416-2XL01-0AB0	02
CPU 417-4	6ES7 417-4XL00-0AB0	01
CPU 417-H	6ES7 417-4HL00-0AB0	01

2 Special Features of STEP 7 Programming with CPUs 41x

Addressing Modules (with CPUs 412 to 416)

The start address of modules and components in either a central configuration or in a distributed configuration must be a value that can be divided by 4 with no remainder (0, 4, 8, 12...).

Starting a Timer

If there is an instruction for starting a timer programmed in the user program, there must be a BCD number at this point in the program sequence in accumulator 1. This also applies if the timer is not started.

Setting a Counter

If there is an instruction for setting a counter programmed in the user program, there must be a BCD number at this point in the program sequence in accumulator 1. This also applies if the counter is not set.

SLD and SRD Instructions (with CPUs 412 to 416)

If parameters 64, 96, 128, 160, 192, or, 224 are transferred to the SRD or SLD instructions in accumulator 2-L-L with the CPUs 41x, status bit CC1 is set.

RND- and RND + Instructions (with CPUs 412 to 416)

If a value in the range 0 to 0.25 is present as a floating-point number, the instruction RND+ supplies the result “0” instead of “1.”
If a value in the range 0 to -0.25 is present as a floating-point number, the instruction RND- supplies the result “0” instead of “-1.”

Writing Bit Instructions (with CPUs 412 to 416)

In the case of a fault, writing bit instructions report a read error instead of a write error. This applies to the following:

- Area length errors (entry in the diagnostic buffer made with event ID W#16#2522 instead of W#16#2523)
- Area errors (entry in the diagnostic buffer made with event ID W#16#2524 instead of W#16#2525)
- I/O access errors (entry in the diagnostic buffer made with event ID W#16#2944 instead of W#16#2945)

I/O Access via Word and Double Word Commands (CPU 417-4 and CPU 417-4H)

With I/O access via word or double word commands, if the first byte or the first one to three bytes exist but the rest of the addressed area does not, accumulator “0” is loaded.

Access to DP Slaves (with CPUs 412 to 416)

A DP station is connected to an S7-400 via an external DP interface module CP 443-5.

If you use word access to access a DP slave with one byte of user data (instructions L PIW, T PQW), the I/O access error organization block (OB122) is not called. After executing the instruction L PIW, accumulator 1 contains B#16#00 instead of the non-existent peripheral byte.

If you use double word access to access a DP slave with three bytes of user data (instructions L PID, T PQD), the I/O access error organization block (OB122) is not called. After executing the instruction L PID, accumulator 1 contains B#16#00 instead of the non-existent peripheral byte.

Single Step (with CPUs 412 to 416)

With the STEP 7 function “single step mode,” the CPU requires more time than the execution time for the instruction. As a result of the scan cycle time monitoring, it is possible that the CPU may go into STOP mode because the cycle time was exceeded. You can avoid this by calling the SFC43 “RE_TRIGR” in the time error organization block (OB80).

Breakpoints (with CPUs 412 to 416)

If you have set a breakpoint at a jump instruction or a block end instruction and the CPU has reached this instruction, neither the function “execute next statement” nor the function “execute call” can be executed. Instead the error message “D063: Resource error: the trigger event is occupied” is displayed.

If you have set a breakpoint at a UC or CC instruction and the CPU has reached this instruction, the function “execute call” cannot be executed. Instead the error message “D063: Resource error: the trigger event is occupied” is displayed.

Remedy: Delete the current breakpoint or move it to the previous command line.

SFC 11 SYNC/FREEZE

SFC11 cannot be called in the startup OBs (OB100, OB101). A call in these OBs is rejected with the RET_VAL identifier 0x80C8. In the other priority classes, you can use SFC11 without restrictions. You can use SFC11 only for the plug-in DP modules (CP 443-5 extended, IM 467). SFC11 cannot be used for the integrated DP interfaces of the CPU 413-2, 412-2, and 416-2.

ET 200M stations assigned to sync/freeze groups with STEP 7 during hardware configuration must not contain FM or CP modules.

Deviation Precision for Time Synchronization

The deviation precision during time synchronization is:

At the communication bus	10 ms
At the MPI	200 ms

Accuracy of the Integrated Real-Time Clock

The accuracy of the integrated real-time clock is:

During operation	8.6 s/d
With battery backup	1.7 s/d

SFC 90 Not Released (CPU 417-4H)

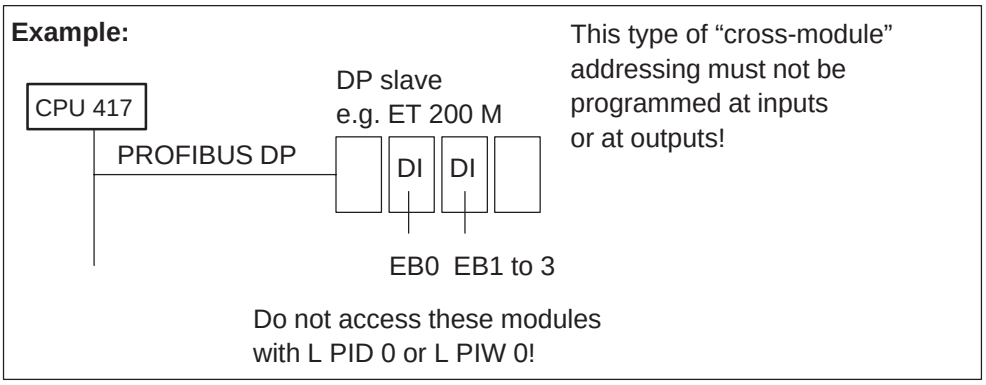
SFC 90 has not yet been released for use with CPU 417-4H.

FM 353/354 Not Distributed (CPU 417-4 and CPU 417-4H)

If you use the CPU 417 as the DP master, you must not use FM 353 and 354 in a distributed configuration within an ET 200M. This applies to:

- FM 353, up to and including 6ES7 353-1AH01-0AE0, firmware version 3.3
- FM 354, up to and including 6ES7 354-1AH01-0AE0, firmware version 3.3

No Cross-Module Addressing in the DP Address Range at the Integrated DP Interface (CPU 417-4 and CPU 417-4H)



4 Special Features of Communication

Number of Operator Stations

This specifies how many operator stations you can log on to the CPU, for example for process control messages.

CPU	OS Stations
CPU 412-1	4
CPU 413-1, CPU 413-2	4
CPU 414-1, CPU 414-2	4
CPU 416-1, CPU 416-2	8
CPU 417-4, CPU 417-4H	8

Communication from PG/OP to Module without MPI

If one of the programming devices or operator panels connected to a multipoint interface (MPI) communicates with an S7-400 module which does not have an MPI connection (for example, SINEC CPs, FM 456 etc.), this module can be reached via the CPU to whose MPI the programming device or operator panel is connected. In this case, the CPU simply acts as an intermediary for the transfer. This type of connection between a programming device or operator panel and a module only communicating via the communication bus occupies two connection resources in the CPU.

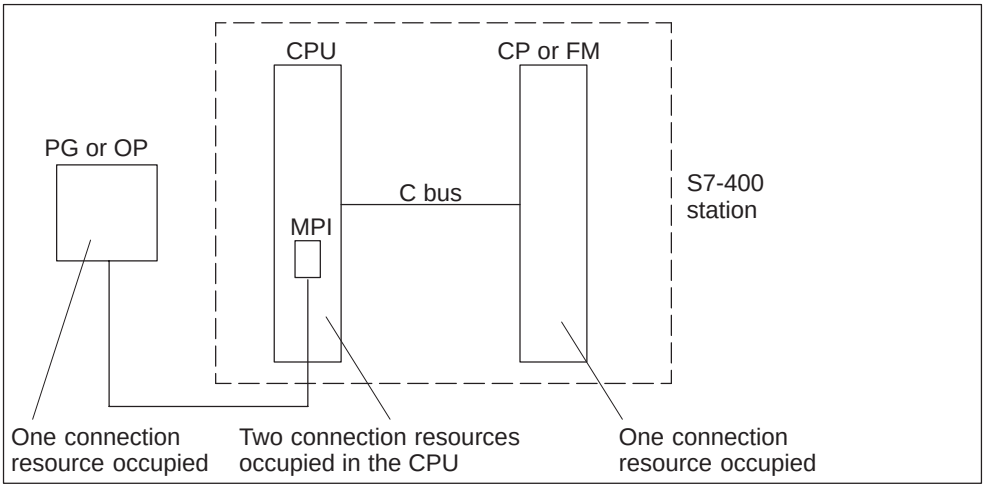


Figure 1-2 Communication between Programming Device/Operator Panel and a Module without MPI

Maximum Number of Connections via MPI

When configuring the connections of a CPU 416 via MPI, remember to include the PG connection in the maximum number of possible connections.

PG Access

A CPU exchanges data with other systems using communication mechanisms, for example with other programmable controllers, with operator interface stations (OP, OS) or with programming devices (see Figure 1-3).

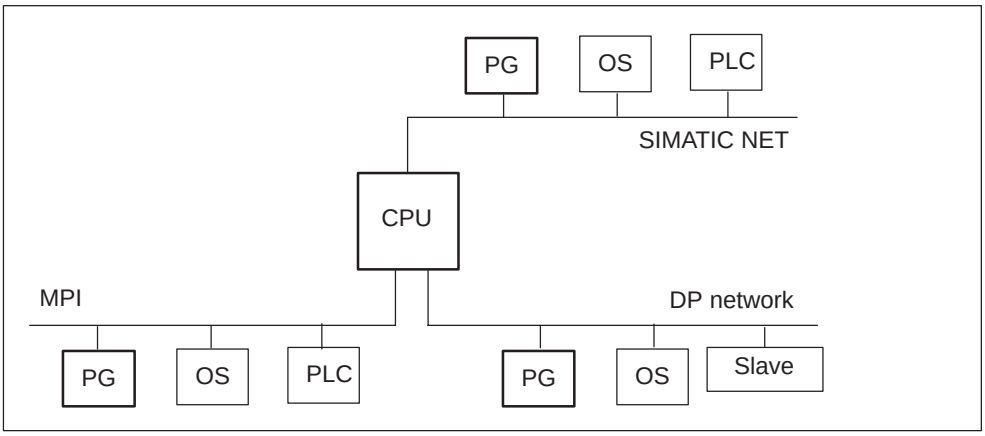


Figure 1-3 Data Exchange

Process communication, including communication services for data exchange between programmable controllers (PLC – PLC) and between programmable controllers and operator interface stations (PLC – OS/OP), has priority in CPUs over communication between programming devices and CPUs.

The CPUs have different characteristics. One of these characteristics is their communication performance. If the communication resources of a CPU are occupied completely by process communication, this can severely hamper access to the CPU from the programming device.

This can often be avoided by a slight reduction in process communication. The following table shows several examples of this. The values relate to a user data length of 200 bytes.

Communication Mechanism	CPU 412, CPU 413		CPU 414, CPU 416	
	Max. No. of Frames	Max. No. of Frames with Reliable PG Access	Max. No. of Frames	Maximum No. of Frames with Reliable PG Access
PLC–PLC communication with USEND/URCV	140 / s	130 / s	150 / s	140 / s
PLC–PLC communication with BSEND/BRCV	100 / s	90 / s	100 / s	90 / s
PLC–PLC communication with AGSEND/RCV *	70 / s	65 / s	70 / s	65 / s
PLC-OP communication (single jobs)	65 / s	60 / s	80 / s	60 / s

* It is advisable to set a minimum scan cycle time of 10 ms or to locate the calls in a cyclic interrupt priority class.

The number of frames per line reflects the performance of the CPU.